MESABI RANGE COMMUNITY & TECHNICAL COLLEGE – VIRGINIA/EVELETH

Course Outline

Course Title:	**Introduction to Digital Logic and Logic Design**	**Submitted By:**	**M. Threapleton**
Semester Course Prefix and Number:	**ENGR 1410**	**Approval Date:**	**April 2002**
Old Quarter Course Prefix and Number:	**PHYS 210**	**Revision Date:**	**April 2002**

Number of Credits: **3**	**Number of Lecture Credits:**	**2**	
Semester(s) Offered:	**Number of Lab Credits:**	**1**	**Number of Lab Hours:** **1**
Negotiated Class Size:	**Number of Studio/Demonstration/Internship Credits:**		

Course Purpose Code:

_____ **0 –** Developmental Courses
_____ **1 –** Non-transferable, General Education
_____ **2 –** Technical course related to career programs
_____ **3 –** College course which has the primary goal of applying certain concepts (e.g. vocal ensemble)
__X__ **4 -** Other college course not considered a part of general education (MNTC) e.g. computer science, health, physical education
_____ **5 –** Course which is intended to fulfill the Minnesota Transfer Curriculum (MNTC) requirements.
_____ **9 –** Continuing Education/Customized Training specialized credit course (not occurring in 0-5)

Catalog Description:
This course is a basic study of the theory and applications of digital electronics. The course includes the study of and-or-not gates, flip-flops, counters, registers, combinational and sequential circuits and their applications to the computer. This course includes an integral laboratory.

Prerequisites and/or recommended entry skills/knowledge:

Course Prerequisite(s):	None
Reading Prerequisite:	None
Composition Prerequisite:	None
Mathematics Prerequisite:	MATH 1521 College Algebra or instructor's consent

Career Programs and Transfer Majors Accessing this Course:
Electrical Engineers and Computer Science

Minnesota Transfer Curriculum Goal(s) partially met by this course if applicable: Notes: No more than two goals may be met by any one course. (Curriculum Committee review and the Chief Academic Officer's approval are required).

0. __X__ None
1. _____ Communications
6. _____ The Humanities and Fine Arts
7. _____ Human Diversity

2. _____ Critical Thinking
3. _____ Natural Sciences
4. _____ Mathematical/Logical Reasoning
5. _____ History and the Social and Behavioral Sciences
8. _____ Global Perspectives
9. _____ Ethical and Civic Responsibility
10. _____ People and the Environment

Learning outcomes, including any relevant competencies listed in the Minnesota Transfer Curriculum:
The student will

1. utilize number systems to perform calculations.
2. explain the fundamentals of Boolean algebra.
3. analyze combinational circuits.
4. plot Karnaugh maps and use the maps in problem analysis
5. design modular systems
6. program PLD's
7. explain flip-flops.
8. analyze sequential logic counters
9. analyze sequential circuits.
10. peform laboratory investigations
11. perform state reduction in specified circuits
12. analyze asynchronous sequential circuits
13. perform PLD design
14. test logic circuits

Student assessment methods:
Standard problem tests and laboratory evaluation, comprehensive design project and comprehensive final examination.

Use of instructional technology (includes software, interactive video and other instructional technologies):
Excel, Mathcad and Mathematica will be used for logic analysis

Outline of the major course content:

I. Number systems and codes
   A. Number systems
   B. Arithmetic
   C. Base conversions
   D. Signed number representation
   E. Computer codes
II. Algebraic methods for the analysis and synthesis of logical circuits
   A. Fundamentals of Boolean algebra
   B. Switching functions
   C. Switching circuits
   D. Analysis of combinational circuits
   E. Synthesis of combinational logic circuits
   F. Computer-aided design of logic circuits
III. Simplification of switching functions
   A. Simplification goals
   B. Characteristics of minimizing methods
   C. Karnaugh maps
   D. Plotting functions in canonical form on the k-map
   E. Simplification of switching functions using k-maps
   F. Product of sums (POS) form using k-maps

G. Incompletely specified functions
H. Using k-maps to eliminate timing hazard
I. Quine-McCluskey tabular minimization method
J. Petrick's algorithm
K. Computer-aided minimization of switching functions

IV. Modular combinational logic
A. Top-down modular design
B. Decoders
C. Encoders
D. Multiplexers/data selectors
E. Demultiplexers/data distributors
F. Binary arithmetic elements
G. Comparators
H. Design example: a computer arithmetic logic unit
I. Computer-aided design of modular systems
J. Simulation of hierarchical systems

V. Combinational circuit design with Programmable Logic Devices (PLD)
A. Semicustom logic devices
B. Logic array circuits
C. Field-programmable logic arrays
D. Programmable read-only memory
E. Programmable array logic
F. Computer-aided design tools for PLD design

VI. Introduction to sequential devices
A. Models for sequential circuits
B. Memory devices
C. Latches
D. Flip-flops
E. Other memory devices
F. Timing circuits
G. Rapidly prototyping sequential circuits

VII. Modular Sequential logic
A. Shift registers
B. Design examples using registers
C. Counters
D. Modulo-N counters
E. Shift registers as counters
F. Multiple-sequence counters
G. Digital fractional rate multipliers

VIII. Analysis and synthesis of synchronous sequential circuits
A. Synchronous sequential circuit models
B. Sequential circuit analysis
C. Synchronous sequential circuit synthesis
D. Incompletely specified circuits
E. Computer-aided design of sequential circuits

IX. Simplification of sequential circuits
A. Redundant states
B. State reduction in completely specified circuits
C. State reduction in incompletely specified circuits
D. Optimal state assigned methods

X. Asynchronous sequential circuits
A. Types of asynchronous circuits
B. Analysis of pulse–mode circuits
C. Analysis of fundamental-mode circuits
D. Synthesis of fundamental-mode circuits

E. Introduction to races, cycles, and hazards

XI. Sequential circuitswith programmable logic devices
   A. Registered programmable logic devices
   B. Programmable gate arrays
   C. Sequential circuit design and PLD device selection
   D. PLD design examples
   E. Computer-aided design of sequential PLDs

XII. Logic circuit testing and testable design
   A. Digital logic circuit testing
   B. Fault models
   C. Combinational logic circuit testing
   D. Sequential logic circuit testing
   E. Built-in self-test
   F. Board and system-level boundary scan

Additional special information (special fees, directives on hazardous materials, etc.)

Transfer Information: (Please list colleges/majors that accept this course in transfer.)
UM, UMD, MSU Mankato, St Cloud State, Michigan Tech, NDSU, UND

Approvals:

Body	Representative Signatures	Date
Curriculum Committee	Kim Giermann	4-2-02
Faculty Association	Georgia Suoja	4-8-02
Meet and Confer	Dr. Jill Peterson	4-17-02
Chief Academic Officer	Dr. Jill Peterson	4-17-02

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